EK

Notice of Allowability	Application No.	Applicant(s)	
	10/721,573	LOONG, LOW YAU	
	Examiner	Art Unit	
	Phallaka Kik	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *Application filed on 11/24/2003, IDS filed on 7/16/2004 and interview on 10/28/2005*.

2. ☒ The allowed claim(s) is/are *1-23*.

3. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 7/16/04
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *20051028* .
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

1. This Office Action responds to the Application filed on 11/24/2003, IDS filed on 7/16/2004, and interview conducted on 10/28/2005. Claims 1-23 are pending. Claims 1-23 have been examined and are allowed, wherein claims 3-5,10,13-14,21,23 are subjected to the following Examiner's Amendment.

EXAMINER'S AMENDMENT

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Babak S. Sani (Reg. No. 37,495) on 10/28/2005.

The application has been amended as follows:

In the claims:

As per **claim 3**, "the shortest" (line 3) has been replaced with --a shortest--; --selected-- has been inserted after "that" (line 4).

As per **claim 4**, --of-- has been inserted after "one" (line 3).

As per **claim 5**, --label-- has been inserted before "maximum" (line 9).

As per **claim 10**, "the maximum" (lines 4-5) has been replaced with --a maximum--.

As per **claim 13**, "the architecture" (line 4) has been replaced with --an architecture--.

As per **claim 14**, "group" (line 6) has been replaced with --groups--.

As per **claim 21**, "the maximum" (line 3) has been replaced with --a maximum--.

As per **claim 23**, "the remaining" (lines 13-14) has been replaced with --remaining--.

Allowable Subject Matter

3. **Claims 1-23** are allowed.

4. The following is an examiner's statement of reasons for allowance:

As per **claims 1-22**, the independent claims 1 and 12, from which the respective claims depend, recite the method/computer system for converting a user design for a programmable integrated circuit into programmable logic blocks (PLBs), comprising the inventive steps/codes for combining, selecting, and combining, involving the use of non-strategic nodes and strategic node, as claimed, wherein the strategic node is defined in Applicant's specification as the "node that is the immediate predecessor of the logic cone's output boundary node, and that does not fanout to any other non-boundary nodes" and the non-strategic node is defined as "a non-boundary node in a logic cone that is not a strategic node" (see Applicant's specification, page 6, paragraph [0044]), which the prior arts made of record failed to teach or suggest. In particular, the prior arts made of record teach various methods/systems for circuit synthesis or mapping to programmable integrated circuits (i.e., for converting a user design for a programmable integrated circuit to a network of programmable logic blocks), including using the combining, cutting, and merging steps/means; however, these combining, cutting and/or merging steps/means failed to make use of the "non-strategic node" and the "strategic

node" in the manner as claimed, as defined in Applicant's specification (see especially **Kale et al.**, US Patent No. 6,594,808, especially col. 7:49 to col. 8, lie 8; col. 9, lines 1-52; **Saucier et al.**, US Patent No. 5,359,537, especially col. 1, lines 34-57; col. 6, lines 18-62; **Kim et al.**, US Patent Application Publication No. 2002/0178432, especially paragraphs [0009] and [0099]; **Chen et al.**, "Performance-Driven Mapping for CPLD Architecture", Proc. ACM/SIGDA International Symposium on Field Programmable Gate Arrays, Monterey, California, February 2001, pp. 39-47, especially sections 2 and 3; **Chen et al.**, "A New Strategy of Performance-Directed Technology Mapping Algorithm for LUT-Based FPGAs", 1996 IEEE International Symposium on Circuits and Systems, Vol. 4, 12-15 May 1996, pp. 822-825, especially section 2; **Yan**, "Logic Synthesis for CPLDs and FPGAs with PLA-Style Logic Blocks", Fourteenth International Conference on VLSI Design, 3-7 January 2001, pp. 291-297, especially section 2; **Chattopadhyay et al.**, "KGPMAP: Library-Based Technology-Mapping Technique for Antifused Based FPGAs", IEE Proceedings of Computers and Digital Techniques, Vol. 141, No. 6, November 1994, pp. 361-368, especially page 326, section 3; **Brasen et al.**, "Using Cone Structures for Circuit Partitioning into FPGA Packages", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 17, No. 7, July 1998, pp 592-600, especially sections II-IV; **Naseer et al.**, "Direct Mapping of RTL Structures onto LUT-Based FPGAs", IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 17, No. 7, July 1998, pp. 624-631, especially sections II, V, and VI(A); **Mathur et al.**, "Compression-Relaxation: A New Approach to Timing-Driven Placement for Regular Architectures", IEEE Transactions on Computer-Aided Design of

Integrated Circuits and Systems, Vol. 16, No. 6, June 1997, pp. 597-608, especially sections III-V; **Cong et al.**, "Simultaneous Depth and Area Minimization in LUT-Based FPGA Mapping", Proceedings of the Third International ACM Symposium on Field-Programmable Gate Arrays, 1995, pp. 68-74, especially sections 3.1 and 3.2; **Francis et al.**, "Chortle: A Technology Mapping Program for Lookup Table-Based Field Programmable Gate Arrays", Proceedings of 27th ACM/IEEE Design Automation Conference, 24-28 June 1990, pp. 613-619, especially section 3.1.4). Accordingly, the claimed invention is novel and un-obvious over the prior arts made of record.

As per **claim 23**, the claim recites the method for converting a user design for a programmable integrated circuit into programmable logic blocks (PLBs), comprising the inventive steps for combining, selecting and combing involving the use of first nodes and second node, wherein the second node is connected directly to an output boundary node of the logic cone and does not fanout to other non-boundary nodes, and the first nodes are the remaining non-boundary nodes in the logic cones, as claimed, which the prior arts made of record failed to teach or suggest. In particular, as indicated in the reasons for the allowance of claims 1-22 above, the prior arts made of record teach various methods/systems for circuit synthesis or mapping to programmable integrated circuits (i.e., for converting a user design for a programmable integrated circuit to a network of programmable logic blocks), including using the combining, cutting, and merging steps/means, and the use of maximum label value in conjunction with the combining steps; however, these combining, cutting and/or merging steps/means failed to make use of the "first nodes" and "second nodes" as further defined in the claim, in

the manner as claimed. Accordingly, the claimed invention is novel and un-obvious over the prior arts made of record.

Conclusion

5. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phallaka Kik whose telephone number is 571-272-1895. The examiner can normally be reached on Monday-Friday, 6:30AM-5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew S. Smith can be reached on 571-272-1907. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any response to this action should be mailed to:

Commissioner for Patents

P. O. Box 1450

Alexandria, VA 22313-145

or faxed to:

571-273-8300

PK
October 28, 2005

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